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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/581,873	06/05/2006	Tim Niggemeier	PD030127	3929

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EXAMINER	
GIARDINO JR, MARK A	

ART UNIT	PAPER NUMBER
2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/581,873	NIGGEMEIER ET AL.	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-14* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 5/27/2009. At this point claims 1-14 have been amended. Thus, claims 1-14 are pending in the instant application.

The instant application having Application No. 10/581,873 has a total of 14 claims pending in the application, there are 2 independent claims and 12 dependent claims, all of which are ready for examination by the examiner.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 4, 6, 7, 10, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mes (US 7,028,142) in view of Zeravleff (US 5,630,096).

Regarding Claim 1, Mes teaches a method for communication between an IC **(processors 104)** and an external RAM **(program memory 102 and arbitration logic 112)**, where the external RAM has at least one memory bank **(Column 6 Lines 17-19, "a single bank is described in this example")** and communication between the IC

and the external RAM is performed via two or more channels **(the multiple channels from the buffer to the arbitration logic in Figure 1A, thus each processor has its own channel)**,

transmitting memory bank commands via multiple channels **(each processor 104 accesses the program memory through the buffers and associated channels as shown in Figure 1A)**;

prioritizing the transmitted memory bank commands the basis of a static priority allocation; **("fetch accesses are preferably given a higher priority than prefetch/data accesses", Column 4 Lines 45-47, also in the last sentence of the abstract, thus fetch accesses are given a statically higher priority over prefetch/data accesses);**

and further prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels **(the channels from the processors use a round-robin fetch arbiter, Column 4 Lines 23-32, thus the commands are given dynamic priority because of the round-robin arbiters 202 and 204 of Figure 2)**.

However, Mes does not explicitly teach where data exchange between the IC and the external RAM necessitates at least two memory bank commands. Zuravleff teaches using multiple commands ("the memory requests are resolved into their required sequences of precharge/bank activate/read-write sequences", where the precharge, activate, and read/write are the commands, Column 5 Lines 2-5).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the at least two memory bank commands of precharge, activate, and read/write commands (as in Zeravleff) for the data exchange between the IC and memory of Mes, as the activate and precharge commands help the RAM process other data commands.

Regarding Claim 3, Mes and Zeravleff teach all limitations of Claim 1, wherein the prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

giving the lowest priority to a channel via which a command has been sent (the round robin arbiter described in Column 4 Lines 23-32 of Mes moves a channel to lowest priority after a command has been sent).

Regarding Claim 4, Mes and Zeravleff meet all limitations of Claim 1, wherein the prioritizing the commands having the same static priority on the basis of a dynamic priority allocation for the channels includes:

giving one of the channels the highest priority in the next clock cycle if this channel does not have the highest priority in the current clock cycle and a command is sent via another channel (the round robin arbiter described in Column 4 Lines 23-32 of Mes moves a channel to highest priority after a different channel sends a command).

Regarding Claim 6, Mes and Zeravleff meet all limitations of Claim 1, wherein the method further includes accessing physically separate memory areas in the external

RAM via the channels (Column 3 Lines 33-36, where an embodiment is shown to use several different memories and thus physically separate memory areas in the external DRAM).

Regarding Claim 7, Mes and Zeravleff teach all limitations of Claim 1, wherein the method further includes accessing jointly used memory areas in the external RAM via the channels and the assurance is given that no successive access operations to a jointly used memory area will arise ("a single wide memory can be used", Column 3 Lines 31-32, thus the processors may use joint areas of memory and to ensure data integrity, successive access operations are obviously limited).

Regarding Claim 10, Mes and Zeravleff teaches all limitations of Claim 1, wherein the method further includes permitting two successive access operations to a memory bank when the access operations are made to the same row in the memory bank (the memory is one bank, Column 6 Line 19-20, and the round robin and static allocation permit successive operations to the memory regardless of the row).

Claim 13 is the memory controller with the same limitations as Claim 1, and is rejected under similar rationale.

Claim 14 is the appliance for reading and/or writing to storage media with the same limitations of Claim 1, and is rejected under similar rationale.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Zeravleff in view of Kuddes (US 5,418,920).

Mes and Zeravleff teach all limitations of Claim 1 as described above. However, Mes and Zeravleff do not specifically teach withdrawing the highest priority of a channel only when this channel can send a command. Kuddes teaches a round robin where a channel is moved to the bottom only if it uses the bus (Column 7 Line 65 to Column 8 Line 12). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have had a channel lose priority only when it can send a command because this ensures that a channel that has not used the bus recently is allowed access to the memory.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Zeravleff in view of Chen et al (US 2003/0051108).

Mes and Zeravleff teach all limitations of Claim 1 as described above. However, Mes and Zeravleff do not teach wherein the method further includes accessing various memory banks via at least one channel by a network. Chen teaches a network (Bank Usage Sorter 110 in Chen) that allows the channels to access any memory bank (paragraph 0014, also see Figure 3 in Chen). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used this network to distribute the memory data evenly across the banks because this reduces costs (see Paragraph 0015 in Chen).

Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Zeravleff in view of Wheeler et al (US 6,983,350).

Mes and Zeravleff teaches all limitations of Claim 1 as described above. However, Mes and Zeravleff do not teach wherein the method further includes always having an access operation to another memory bank effected between two access operations to a memory bank. Wheeler teaches alternating memory banks (Column 5 Lines 33 to 42 in Wheeler, alternating between an even and odd memory bank places at least one access operation between each bank).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to arrange memory operations in such a way. Wheeler provides the motivation when he states that the bandwidth of the RAM is improved (Column 5 Lines 40-42 in Wheeler).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Zeravleff in view of LaBerge (US 2001/0044885).

Mes and Zeravleff teach all limitations of Claim 1 as described above. However, Mes and Zeravleff are silent on depicting the states of the memory banks by associated state machines. LaBerge teaches a memory bank that has a state machine (containing at least the states 'idle' and 'not idle', see Paragraph 0023 and Figure 8 in LaBerge). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used a state machine to control the memory banks because tracking idle states results in reducing latency incurred between successive memory operations (see Paragraph 0019 in LaBerge).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mes and Zeravleff in view of the power point entitled "Random Access Memory".

Mes and Zeravleff teaches all limitations of Claim 1 as described above. However, Zeravleff does not teach further including a plurality of RAM modules and transmitting a chip enable signal in order to select the desired module. "Random Access Memory" teaches combining several RAM modules into a single RAM module and a chip enable signal (called chip select in the power point) to select the desired module (see Slides 17 and 18). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to which the subject matter pertains to have combined the RAM modules this way because it allows for larger memories to be made (see Slide 18 in "Random Access Memory").

ARGUMENTS CONCERNING NON-PRIOR ART REJECTIONS/OBJECTIONS

Specification Objections

Applicant's arguments/amendments with respect to the specification have been considered and have overcome the Examiner's prior objections and thus are withdrawn.

Rejections - USC 112

Applicant's arguments/amendments with respect to claims 1-14 have been considered and have overcome the Examiner's prior rejections and thus are withdrawn.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments with respect to claim 1 and 13 that Mes does not teach "data exchange between the IC and the external RAM necessitates at least two memory bank commands" has been considered but is moot in view of the new grounds of rejection.

However, the examiner notes that the claims do not specifically draw a distinction between an "instruction" and a "command" as argued on Page 13. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). One of ordinary skill in the art would reasonably interpret a read or write operation (as in the processors to the memory in Mes) a "memory bank command".

Further, the "at least two memory bank commands" described in the preamble of claim 1 are not specifically referred to in the body of the claims, as the limitation "transmitting memory bank commands" does not refer to the memory bank commands recited previously. Therefore, the commands in the preamble and the commands in the body of the claim can be interpreted as different commands in the broadest reasonable interpretation.

CLOSING COMMENTS

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

SUBJECT MATTER CONSIDERED ALLOWABLE

Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1 and 3-14 have received a second action on the merits and are subject of a second action final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571)

270-3565 and can normally be reached on Monday - Thursday 7:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272 - 4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

August 13, 2009

/Stephen Elmore/
Primary Examiner, Art Unit 2185